Electronic Fluorescent Ballast using a Power Factor Correction Techniques for Loads Greater than 300 Watts

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ABSTRACT

This paper describes various power factor schemes used to correct power factor in electronic ballast or other types of power supplies. The power inverter used for the fluorescent lamp load is a Current Fed Sine Wave Inverter while the unique power factor correction and dimming is accomplished with a boost approach. Keeping the inverter the same, several historical passive techniques were designed, built, and tested; these results are to be used as a bench mark against the active power factor circuit topologies. The results are given for a matrix of low, normal and high line voltages of a 4 lamp load greater than 300 watts.

POWER INVERTER "CURRENT FED SINE WAVE"

A power inverter was built to power four or more fluorescent lamps to be used in horticulture in conjunction with hydroponics. The lamps were the F96T12HO type which are a rapid start type. The lamps require 800 milliamperes to operate and are specified to have 110 arc watts at 60 Hertz. Due to the greater efficiencies of operating the lamps at high frequencies arc current requirements are reduced to 600 milliamperes. Light output was not measured but the arc watts, arc current, and arc voltage were measured along with the input wattage. Input watts were monitored to be sure that greater than 300 arc watts were delivered to the load at nominal line voltages.

The current fed sine wave inverter was chosen over the series resonant topology because the current fed system is stable under open circuit and short circuit conditions and special feedback for protection under open circuit conditions was not needed (1,2). Open circuit conditions occur during relamping for example, the old lamps are removed and new ones replaced. This occurs while the AC line voltage is applied to the ballast.

Capacitor ballasting is used with series connected lamps. Two of these are paralleled to operate four lamps (Figure 1). Capacitor ballasting was chosen rather than the inductive system because of its simplicity and cost effectiveness.

This system provides an acceptable sine wave voltage and current to the lamps. When the input DC voltage to the power inverter is varied, the arc current is also varied and thus a dimming system is possible.

POWER FACTOR CORRECTION

Different power factor correction schemes were built and tested using incandescent lamp loads to prove the circuits. Afterwards the inverter ballast was used as the load. The goal was to have a power factor greater than 90%, third order harmonic less than 27% of the fundamental, and a Total Harmonic Distortion (THD) of current draw of less than 32%. These are the limits defined by the standard IEC 555-2 for luminaries. The value of 32% was obtained by using the square root of the sum of the harmonics listed below; the power factor was set to be greater than 90%. The standard has the following specifications:

HARMONIC	PERCENT VALUE OF CURRENT
2	2%
3	30% X (power factor)
5	10%
7	7%
9	5%
$11 \le N \le 39$	3%

The different power factor circuits used are shown in Figures 2 through 7. Figures 1, 2, 3, 4, and 5 (3) are passive while Figure 8 and 9 are active.

CURRENT HARMONIC DISTORTION CALCULATION

The technique used to calculate harmonic distortion is as follows:

$$\text{Total Harmonic Distortion} = \text{T.H.D.}$$

$$\text{T.H.D.} = \frac{\sqrt{I^2_{\text{rms total}} - I^2_{\text{fundamental}}}}{I_{\text{fundamental}}}$$

CH2992-6/91/0000-0393 $1.00

The currents, volts, wattages, and power factor are measured with a electronic Power analyzer from Voltech; models PM 1000 and PM 3000 were used. The $I_{rms\ total}$ is the total input line current with all of its harmonics. The $I_{fundamental}$ is the 60 Hertz component of the fourier analysis performed by the instrument. In some cases the phase angle is recorded which is referenced to the ac line voltage zero crossing.

The above technique works well as long as the distortion is above 5 percent. When the distortion reaches the 5 percent or smaller, the $I_{fundamental}$ and the $I_{rms\ total}$ are nearly identical. In some cases the instruments have had the $I_{rms\ total}$ smaller than the $I_{fundamental}$. This occurs because of the ac line fluctuations; a ac voltage line stabilizer was unavailable. In all cases recorded, the distortion was greater than 5 percent.

This method should give the same answer as a distortion analyzer provided the number of digits and the frequency response is sufficient. A reverification of the measurements was performed by using a second method to determine the Total Harmonic Distortion. The technique was the square root of the sum of the squares of the harmonics.

Both of these methods are presented because an Hewlet-Packard analog distortion analyzer was not available at the time. It can be seen there is a small difference between the readings. Some of the difference can be explained by the fact that there was no stable line voltage source. Second, the variac and isolation transformer added a voltage distortion which adds to the current distortion.

A third method to check on the distortion would be an audio Spectrum Analyzer with a 20 Hertz lower frequency limit. The Spectrum analyzer approach would use the square root of the sum of the squares. This is described below.

Total Harmonic Distortion = T.H.D.

$$T.H.D. = \sqrt{\sum 2nd^2+3rd^2+5th^2+7th^2+\ldots}$$

2nd = 120 Hz percent component
3rd = 180 Hz percent component
5th = 300 Hz percent component

PASSIVE TECHNIQUES

No Power Factor Circuit

The base of the entire measurement is an unpower factored system operating four lamps. The base schematic is shown in Figure 1. The data gathered is indicated in Table 1. As can be seen, the power factor is poor but it would be much worse if an isolation transformer and variac were not used. Note that the distortion is extremely high with very large harmonic content.

To obtain a better understanding of what kind of harmonics are present in the line when the load is near the distribution panel (Stiff Line), an experiment was performed using Figure 2. Data is presented in Table 2. Note the high value of the harmonics. It is interesting to note the power factor is approximately 58%.

LC Filter Before Bridge

In Figure 3, the inductor and capacitor are before the bridge rectifies. This is presently used by electronic ballast manufacturers in some of their products. A complete set of data was collected to have an understanding of what type of power factor can be obtained. Different value chokes and film capacitors were tested using different incandescent lamp loads. Data was recorded to obtain the best values of both power factor and harmonic distortion.

A study of the data has revealed that there are two conditions that must be met in order to have acceptable results. The first condition sets the open circuit voltage. The second condition maintains the DC voltage to the electrolytic capacitor that supplies energy to the load.

CONDITION ONE

The resonant frequency of the input in inductor and the film capacitor should be greater than three time the line frequency. For 60 Hz operations this means greater than 180 Hz. In the test conditions, 185 Hz worked satisfactorily.

$$F_r = \frac{1}{2\pi\sqrt{LC}}$$

$$3 \times \text{Line Freq.} \leq F_r$$

CONDITION TWO

The load impedance Z_l should be greater than the characteristic impedance of the input inductor and input film capacitor.

$$Z_l = \frac{V_l}{I_l}$$

$$Z_o = \sqrt{\frac{L_{input}}{C_{film}}}$$

$$Z_l > Z_o$$

Z_l Load impedance
V_l DC Load voltage
I_l DC Load current
Z_o Characteristic Impedance

The test results using the ballast circuit of Figure 1 were again recorded. The data is shown in Table 3. Because the inductors were of the 120 volt type, a voltage double rectification had to be used in order not to saturate the inductors. The inductors used were actually reactor ballasts for 150 watt High Pressure

Sodium Lamps. They were rated for 120 Volts and 3 Amps.

LC Filter After Bridge

Another method of obtaining power factor is to place the LC filter network after the bridge (Figure 4). In this case, the inductor carries current and must be designed with a large air gap. It was found that this circuit was more critical than the LC filter before the bridge. The size of the inductor was the same for both cases. In fact the inductor was the same, made of two inductors in parallel, measuring 40 millihenries under power AC conditions. The value of the capacitor was measured at 8.3 uF which was a 1.5 uF plus a 6.8 uF; both capacitors had a 400 VDC rating. This power factor circuit approach was tested on the AC line using a variac and isolation transformer to gather the data at the various line voltages. The ballast capacitor was adjusted in order to have the lamps powered to greater than 300 Arc watts. The data is presented in Table 4.

The total harmonic distortion is greater in this approach than the approach with the inductor-capacitor in front of the bridge. It can be determined that the cost of the inductor is the same with both approaches but the capacitor cost is more with the LC filter in front of the bridge.

RIPPLED POWER FACTOR CIRCUIT

The rippled power factor circuit is some times referred to as a **"VALLEY FILL"** approach. This rippled power factor circuit has several forms and develops the following voltage wave form as can be seen in Figure 5. There are methods to obtain the waveform; the math of power factor was described in paper published in 1985 at PCIM (3). The power factor can be expected to be 95%. Similarly because of the inductance and resistance of the variac and isolation transformer the peak of the current is 80% small than a stiff line. Table 5 is the collection of data. This does give a power factor of greater than 90 percent, but the harmonic content is larger than what the IEC 555-2 proposed standard would allow. To lower the current spike which charges the electrolytic capacitor, an inductor is added in two locations and the results are indicated as follows.

VALLEY FILL INDUCTOR IN CHARGING LEG

The first location to add the inductor is in the charging leg as indicated in Figure 6. The inductor is a EE75 powered iron core having a cross-sectional area, A_e, of 3.62 cm^2. The inductor was wound and tested using the Power Analyzer with 1 amp of 60 Hertz current. The inductance value was calculated to be 24 millihenries. This is a power measurement rather than a small signal measurement that most RLC bridges make. This was done because of the property that powered iron exhibits between its initial permeability of low flux and its power permeability of high flux.

Data was collected and summarized in Table 6. As in the other data recorded, an isolation transformer and variac was used. The voltage harmonic distortion was noted to be 3.7 percent. This influence should be noted and taken into account when reanalyzing the data. To see if the placement of the choke has any effect, the choke was moved in front of the bridge rectifier.

VALLEY FILL INDUCTOR IN FRONT OF BRIDGE

As indicated the 24 millihenry inductor was placed in front of the bridge rectifier. This can be see in Figure 7. This placement has more advantages than the location just in the charging leg. The following three advantages are listed:

1. Limit the in-rush current during power up
2. Provide limited EMI filtering if split and wound on both power input legs. (No EMI specifications or limits were considered in this paper)
3. Limit the peak current during the charging of the electrolytic capacitors.

The circuit shown in Figure 7 was tested using the sine wave inverter. The data was collect and can be seen in Table 7. The ac line was varied using a variac and a isolation transformer was used in order to obtain the 270 volts. Again the input voltage and input current was recorded.

When comparing the circuit test results to the IEC standard, this circuit gives better results. The Total Harmonic Distortion is within the limits but the individual harmonics are exceeding the limits imposed. The size of the inductor would have to be increased to two times or approximately 50 milliheneries.

ACTIVE POWER FACTOR

Most of the active power factor circuits presented in the literature today use the boost converter. There are commercial integrated circuits from many semiconductor manufacturers for this purpose. A partial list include the following: Siemen's TDA 4814; Unitrode's UC 3854, Silicon General's SG 3561 and Micro-Linear's ML 4812 and ML 4813. The TDA4814 and SG 3561 are specified for electronic ballast applications while the UC 3845, ML 4812, and ML 4813 are for the power supply industry.

This paper uses another standard Pulse Width Modulator Integrated Circuit the UC 3842A in a boost configuration. To compensate the loop, a slope compensation circuit is used.

ACTIVE BOOST CONVERTER

The active power factor boost converter circuit was built and tested (Figure 8). This circuit has several items of interest: first the slope compensation, second the over voltage protection, and third the integration of the current. The boost converter was then married to the

Current Fed Sine Wave Inverter and numerous test were run. Three of the test runs are shown in Table 8. At the bottom of each section in Table 8 are the IEC specifications. In the first test, the bus voltage was set to 340 volts and the ballast capacitors adjusted to give the greatest output load of 400 arc watts. The range of input voltage was limited due to the low output voltage.

The second set has a DC output voltage at 385 volts. The output ballast capacitors were adjusted downward to give a lower output current. The Arc wattage in the lamps was maintained at 300 watts.

The last set of data the bus voltage was set at 400 volts DC. This test set has the greater range of input voltage recorded from 180 volts to 250 volts rms at 60 Hertz. The ballast capacitors were the same as the test above and as can be seen the output arc wattage does increase about 10 watts per lamp.

Higher input voltages were not tested here because the isolation transformer and variac started to hum. It was believed that the voltage limits of the isolation transformer had been reached and due to high voltage produced a hum.

CONCLUSION

The advantage of the first passive LC power factor correction technique is its simplicity and ease of implementation. The major disadvantages are the size of the components and the hum that has to be overcome. There are two different types of hum. The first hum is the transformer hum that is composed of laminations and windings. These can be reduced by good manufacturing techniques like varnish. The second type of hum is in the film capacitors. If the film capacitors are not manufactured with good sealed outer shell, the foil vibrates. There are special types of capacitors for this application which are more expensive.

The valley fill approach is cost effective, but the output of the DC bus has a ripple of two times the line frequency. This ripple produced an arc current ripple that causes the light produced by the lamps to have a flicker similar to the magnetic type ballast. When the powered iron choke was added to the valley fill circuits, a hum was produced. This inductor must be properly manufactured to eliminate the hum.

The active boost was easy to build and use after the limitations were understood. The limitations include the input supply voltage range which must be maintained with a certain range. This AC supply input has an upper limit that is defined by the output DC bus voltage. The lower limit is defined by the peak current. This current is sensed by the resistor in the source leg to ground. Lowering the value of this resistor would lower the AC supply input voltage. The size of the boost converter including the inductor was the size of one of the two chokes used in the passive LC circuit approach. The boost converter choke did not hum even though it was not varnished. The choke was wound on a simple bobbin ferrite core.

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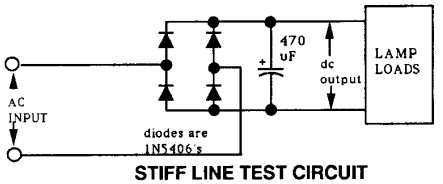
(2) Michael Bairanzada, (edited) Jim Spangler, "The Electronic Control of Fluorescent Lamps," Motorola Application Note AN1049.

(3) Jim Spangler, "A Power Factored Corrected MOSFET, Multiple Output, Flyback Switching Supply," Proceedings 10th PCIM '85 Conf. Oct 85, pp.19-32.

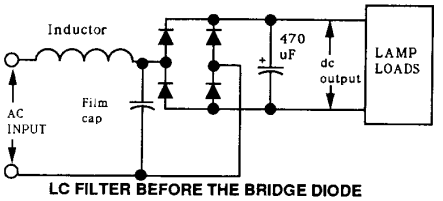
ACKNOWLEDGEMENTS

(1) Dave Pacholok for use of his Voltech PM 1000 and help with the Boost Converter. He provided the ferrite drum cores for the Boost and Litz wire for the Inverter output transformer.

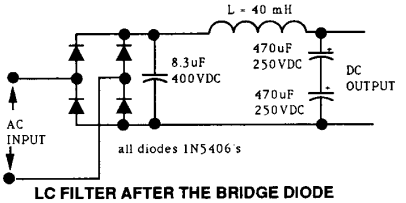
(2) Jack Christiensen of Berndt Assoc. for loaning the demo Voltech PM 3000 used to obtain the output lamp wattages measurements and phase angle measurements of the harmonic currents.



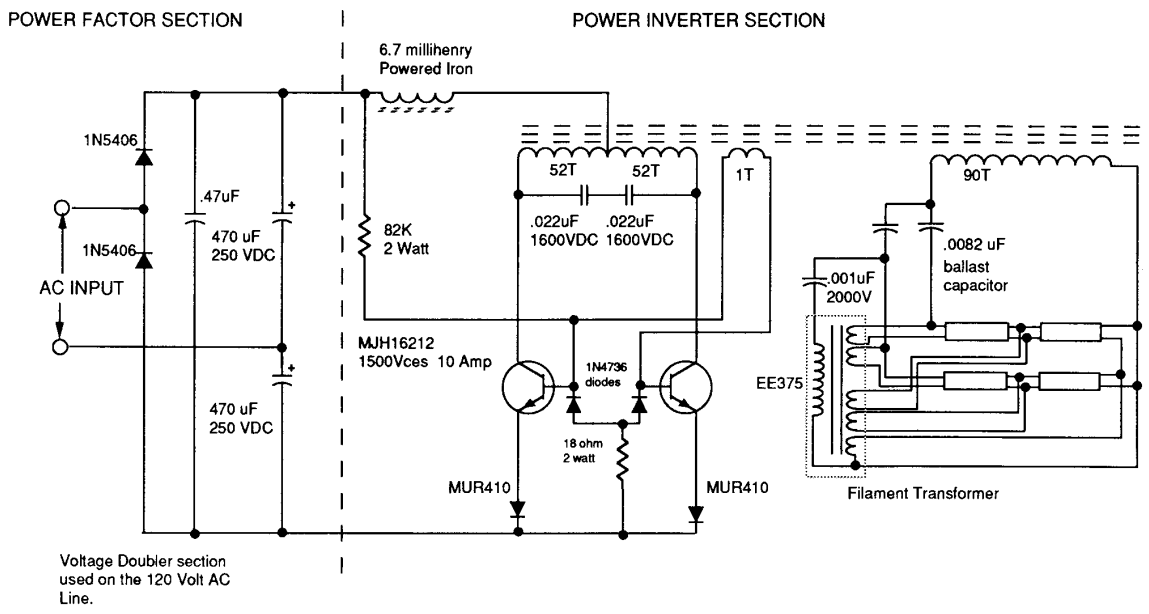
STIFF LINE TEST CIRCUIT
Figure 2



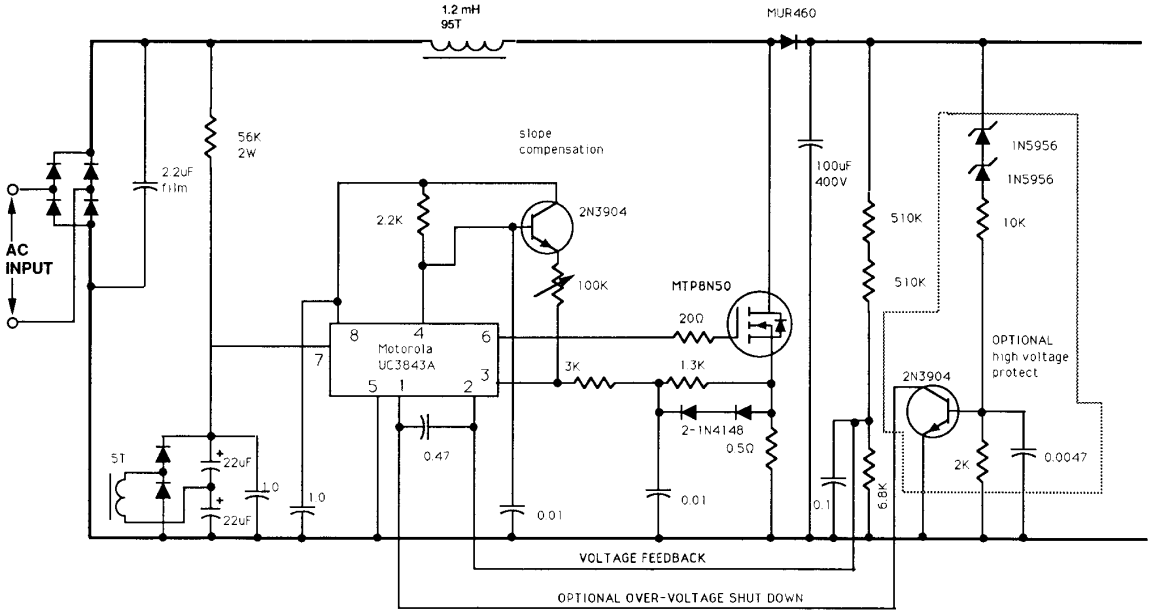
LC FILTER BEFORE THE BRIDGE DIODE
Figure 3



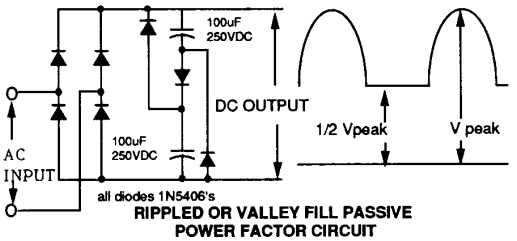
LC FILTER AFTER THE BRIDGE DIODE
Figure 4



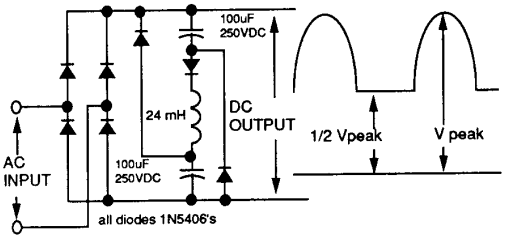
CURRENT FED SINE WAVE CONVERTER
FIGURE 1



CONSTANT FREQUENCY VERSION
FIGURE 8

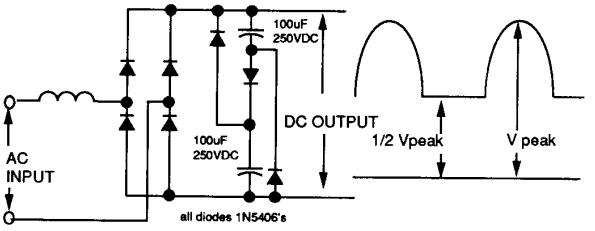


RIPPLED OR VALLEY FILL PASSIVE POWER FACTOR CIRCUIT
FIGURE 5



RIPPLED POWER FACTOR WITH INDUCTOR IN CHARGING LEG

FIGURE 6



RIPPLED POWER FACTOR WITH INDUCTOR IN SERIES WITH THE LINE
FIGURE 7

TABLE 1
Diode Bridge No Filter

volts	amps	watts	pwr factor	fund	these are in per cent							T.H.D.	
					2nd	3rd	5th	7th	9th	11th	13th		
249.7	2.385	418.4	-0.701	1.7613	0.30	77.44	42.95	11.37	7.93	11.01	5.47	91.30	90.32
267.3	2.367	443.8	-0.703	1.7516	0.40	77.20	42.49	11.75	8.11	10.40	4.91	90.89	89.89
282.6	2.3318	462.9	-0.708	1.7267	0.31	76.64	41.66	11.74	8.56	9.50	4.04	90.76	88.96
		IEC SPECIFICATIONS			2.00	27.00	10.00	7.00	5.00	3.00	3.00		32.28

TABLE 2
Stiff Line Power Factor and Harmonic Data

volts	amps	watts	pwr factor	fund	these are in per cent							T.H.D.	T.H.D.
					2nd	3rd	5th	7th	9th	11th	13th		sum of sq
122.48	1.803	127.7	-0.578	1.070	0.84	91.10	74.71	54.36	33.05	14.37	2.85	135.62	134.67
122.28	1.943	138.5	-0.583	1.170	0.58	90.43	72.92	51.38	29.52	11.28	3.75	132.58	130.90
		IEC SPECIFICATIONS			2.00	27.00	10.00	7.00	5.00	3.00	3.00		32.28

TABLE 3
L C Filter in front of Diode Bridge: Voltage Doubler 40 mH & 20.4uF

volts	amps	watts	pwr factor	fund	these are in per cent							T.H.D.	T.H.D.
					2nd	3rd	5th	7th	9th	11th	13th		sum of sq
108.06	3.117	315.7	0.945	3.034	0.09	21.32	4.31	1.48	0.56	0.21	0.22	23.55	22.02
120.18	3.360	377.7	0.938	3.276	0.11	21.94	4.40	1.63	0.41	0.17	0.25	22.79	22.68
132.40	3.540	436.6	0.924	3.437	0.10	23.37	4.51	1.56	0.37	0.20	0.22	24.66	24.10
		IEC SPECIFICATIONS			2.00	27.00	10.00	7.00	5.00	3.00	3.00		32.28

TABLE 4
L C Filter After Diode Bridge

volts	amps	watts	pwr factor	fund	these are in per cent							T.H.D.	T.H.D.
					2nd	3rd	5th	7th	9th	11th	13th		sum of sq
251.2	1.594	365.6	-0.910	1.467	0.33	27.42	21.72	6.03	11.81	5.01	9.17	42.48	37.77
267.6	1.641	399.2	-0.909	1.504	0.34	27.69	22.18	6.80	12.26	5.40	10.03	43.61	38.56
284.1	1.688	434.5	-0.906	1.542	0.27	28.23	22.65	7.80	13.10	6.07	11.75	44.50	39.77
		IEC SPECIFICATIONS			2.00	27.00	10.00	7.00	5.00	3.00	3.00		32.28

TABLE 5

Valley Fill No Inductor to Limit Current

volts	amps	watts	pwr factor	fund	these are in per cent 2nd	3rd	5th	7th	9th	11th	13th	T.H.D.	T.H.D. sum of sq
250.3	1.218	285.6	-0.936	1.155	0.33	29.25	4.36	6.41	11.78	7.75	2.49	33.54	33.41
268.7	1.313	336.6	-0.953	1.255	0.33	22.45	9.90	10.48	9.19	8.66	1.40	30.75	29.55
285.6	1.378	377.1	-0.955	1.331	0.21	20.57	12.96	11.04	8.87	9.84	2.50	26.61	29.84
		IEC SPECIFICATIONS			2.00	27.00	10.00	7.00	5.00	3.00	3.00		32.28

TABLE 6

Power Choke in the Charging Path

volts	amps	watts	pwr factor	fund	these are in per cent 2nd	3rd	5th	7th	9th	11th	13th	T.H.D.	T.H.D. sum of sq
253.0	1.195	283.3	-0.939	1.135	0.15	28.88	7.54	1.02	8.25	4.62	6.17	32.94	31.35
265.5	1.254	315.7	-0.950	1.199	0.19	24.46	10.61	1.51	7.59	3.86	6.35	30.40	28.06
282.0	1.303	354.1	-0.958	1.267	0.18	20.40	14.31	3.55	5.97	4.46	5.54	23.98	26.28
		IEC SPECIFICATIONS			2.00	27.00	10.00	7.00	5.00	3.00	3.00		32.28

TABLE 7

Power choke in front of valley fill

volts	amps	watts	pwr factor	fund	these are in per cent 2nd	3rd	5th	7th	9th	11th	13th	T.H.D.	T.H.D. sum of sq
257.5	1.2681	296.4	-0.925	1.206	0.19	29.98	1.48	5.14	8.31	5.60	1.77	32.50	32.11
268.4	1.3621	345.3	-0.946	1.311	0.27	24.27	4.90	5.36	8.90	4.91	3.13	28.19	27.48
282.7	1.4263	383.8	-0.953	1.377	0.20	21.91	8.37	7.74	8.22	4.96	3.88	27.00	26.78
		IEC SPECIFICATIONS			2.00	27.00	10.00	7.00	5.00	3.00	3.00		32.28

TABLE 8

Boost Conveter Power Factor Measurements

340 VOLT BUS

volts	amps	watts	pwr fact	fund	these are in percent 2nd	3rd	5th	7th	9th	V out dc bus	T.H.D. %	T.H.D. sum of sq.	W lamps1	W lamps2
181.1	2.410	422.0	0.970	2.356	0.12	17.23	10.00	5.72	2.96	322.0	21.53	20.94	197.5	165.8
190.6	2.419	445.3	0.970	2.364	0.02	17.61	9.93	5.86	3.25	328.8	21.70	21.30	204.0	181.5
199.6	2.417	469.1	0.968	2.360	0.09	18.14	9.80	6.03	3.49	338.8	22.11	21.76	213.2	195.5
210.0	2.267	466.0	0.971	2.223	0.09	17.09	9.09	6.00	3.80	338.9	19.99	20.62	213.3	195.6
220.3	2.156	463.0	0.974	2.109	0.06	15.86	8.33	5.73	3.83	338.9	21.23	19.19	213.3	195.3
230.9	2.038	460.5	0.978	2.005	0.10	14.05	7.08	5.32	3.61	338.9	18.22	17.00	213.1	195.6
		IEC SPECIFICATIONS			2.00	27.00	10.00	7.00	5.00			32.00		

385 VOLT BUS

volts	amps	watts	pwr fact	fund	these are in percent 2nd	3rd	5th	7th	9th	V out dc bus	T.H.D. %	T.H.D. sum of sq.	W lamps1	W lamps2
182.3	1.950	348.0	0.972	1.907	0.05	16.19	10.19	5.85	2.96	384.3	21.36	20.22	163.7	137.3
190.0	1.897	350.9	0.973	1.864	0.06	15.63	10.00	5.81	3.18	384.1	18.90	19.70	163.1	138.0
199.4	1.795	349.8	0.976	1.769	0.08	14.00	9.27	5.80	3.35	384.0	17.21	18.08	163.1	139.5
211.1	1.684	348.8	0.980	1.663	0.03	11.53	8.27	5.40	3.36	384.0	15.94	15.55	162.8	140.0
220.2	1.603	348.1	0.982	1.583	0.16	9.26	7.28	4.83	3.00	383.8	16.03	13.08	162.6	140.0
231.0	1.530	347.2	0.985	1.515	0.17	6.94	6.25	4.28	2.74	383.7	13.91	10.63	162.6	140.4
240.6	1.463	347.1	0.986	1.459	0.19	4.58	5.22	3.65	2.26	383.6	7.41	8.17	162.3	140.2
		IEC SPECIFICATIONS			2.00	27.00	10.00	7.00	5.00			32.00		

400 VOLT BUS

volts	amps	watts	pwr fact	fund	these are in percent 2nd	3rd	5th	7th	9th	V out dc bus	T.H.D. %	T.H.D. sum of sq.	W lamps1	W lamps2
180.0	2.163	377.8	0.966	2.119	0.16	18.67	10.88	5.61	2.45	397.8	20.48	22.46	172.0	151.0
190.0	2.049	376.6	0.969	2.001	0.13	17.57	10.62	5.90	2.93	397.5	22.03	21.56	171.0	151.0
200.6	1.915	374.1	0.973	1.874	0.06	15.95	9.95	6.02	3.38	397.5	21.03	20.03	171.0	151.0
210.8	1.810	372.2	0.976	1.780	0.02	14.40	9.18	5.82	3.57	397.4	18.44	18.39	171.0	151.0
221.1	1.710	371.2	0.978	1.689	0.09	12.18	8.24	5.38	3.53	397.3	15.82	16.05	171.0	151.0
229.6	1.637	370.1	0.981	1.622	0.07	10.64	7.45	5.01	3.46	397.3	13.63	14.35	171.0	151.0
239.6	1.563	369.0	0.983	1.553	0.19	8.47	6.40	4.47	3.00	397.4	11.37	11.90	171.0	151.0
250.0	1.500	369.00	0.984	1.490	0.24	6.43	5.36	3.82	2.64	397.4	11.61	9.58	171.0	151.0
		IEC SPECIFICATIONS			2.00	27.00	10.00	7.00	5.00			32.00		